MC10170

9+2-Bit Parity Generator/ Checker

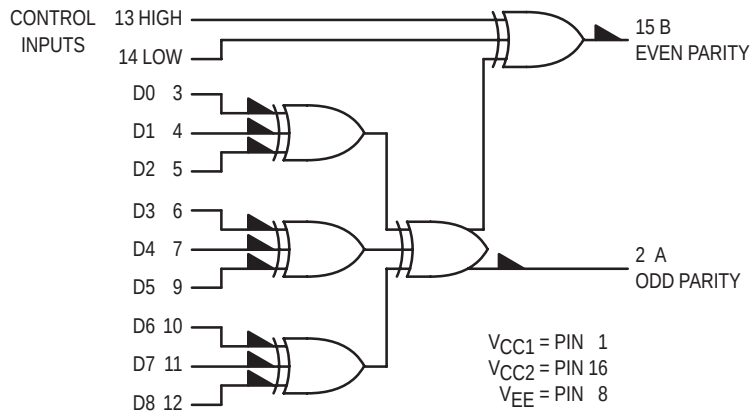
The MC10170 is a 11–bit parity circuit, which is segmented into 9 data bits and 2 control bits.

Output A generates odd parity on 9 bits; that is, Output A goes high for an odd number of high logic levels on the bit inputs in only 2 gate delays.

The Control Inputs can be used to expand parity to larger numbers of bits with minimal delay or can be used to generate even parity. To expand parity to larger words, the MC10170 can be used with the MC10160 or other MC10170's. The MC10170 can generate both even and odd parity.

- P_D = 300 mW typ/pkg (No Load)
- t_{pd} = 2.5 ns typ (Control Inputs to B Output)
  4.0 ns typ (Data Inputs to A Output)
  6.0 ns typ (Data Inputs to B Output)
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



INPUTS	OUTPUTS	
Sum of D Inputs at High Level	Odd Parity	Even Parity
	Output A	Output B
Even	Low	High
Odd	High	Low

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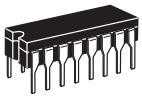
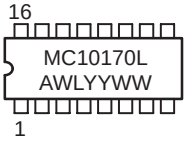
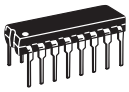
MARKING DIAGRAMS

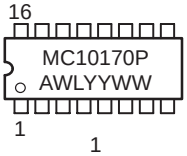


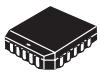
CDIP–16
L SUFFIX
CASE 620



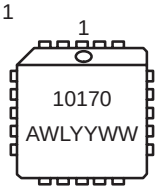


PDIP–16
P SUFFIX
CASE 648



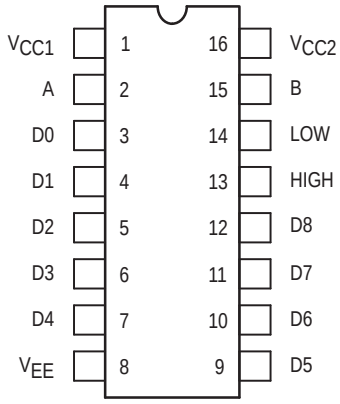


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10170L	CDIP–16	25 Units / Rail
MC10170P	PDIP–16	25 Units / Rail
MC10170FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		78		57	71		78	mAdc
Input Current	I_{inH}	3 5		350 350			200 220		220 220	μAdc
	I_{inL}	3	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 15	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 15	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 15	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 15		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{13+15+} t_{14-15-} t_{3+2-} t_{3-15+}	15 15 2 15	1.5 1.5 2.0 4.0	4.2 4.2 6.6 9.5	1.5 1.5 2.0 4.0	2.5 2.5 4.0 6.0	4.0 4.0 6.0 8.8	1.5 1.5 2.0 4.0	4.4 4.4 6.6 9.5	
Rise Time (20 to 80%)	t_{2+}	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	
Fall Time (20 to 80%)	t_{2-}	2	1.5	4.3	1.5	2.0	3.9	1.5	4.3	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8						1, 16
Input Current		I_{inH}	3 5	3 5				8 8	1, 16 1, 16
		I_{inL}	3		3			8	1, 16
Output Voltage	Logic 1	V_{OH}	2 15	3, 4, 5 14				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	2 15	4, 5 13, 14				8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	2 15			5 13		8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	2 15				5 13	8 8	1, 16 1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0**
Propagation Delay		t_{13+15+}	15			13	15	8	1, 16
		t_{14-15-}	15			14	15	8	1, 16
		t_{3+2-}	2			3	2	8	1, 16
		t_{3-15+}	15			3	15	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2			3	2	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2			3	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.